IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Eduard F. Stikvoort et al.	CONFIRMATION NO.: 3883 DOCKET NO.: NL031244 US1
SERIAL NO.:	10/576,554	EXAMINER: Tuan T. Lam
FILED:	April 19, 2006	ART UNIT: 2816
FOR:	FREQUENCY DIVIDER	

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Commissioner for Patents
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DO NOT ENTER: /TL/ (07/31/2008)

AMENDMENT AFTER FINAL REJECTON

Dear Sir:

In response to the Final Office Action dated July 17, 2008, please amend the application as follows:

IN THE CLAIMS:

1. (Currently Amended) A frequency divider comprising:

a first flip-flop without stacked transistors having a first clock input for receiving a clock signal, the first flip-flop further comprising a first set input and a first non-inverted output; and

a second flip-flop without stacked transistors having a second clock input for receiving a second clock signal that is substantially in anti-phase with the clock signal inputted into the first clock input, a second set input coupled to the first non-inverted output, a second non-inverted output and a second inverted output, wherein the second inverted output is coupled to the first set input for providing an inverted output signal from said second non-inverted output of the second flip-flop as feedback to the set input of the first flip-flop; and

wherein said frequency divider does not have an additional controlled inverter for providing a time delay.

2. (Previously Presented)A frequency divider as claimed in claim 1, wherein a period of the second clock signal is of the same order of magnitude as a delay through the second inverted output of the divider.

3. (Currently Amended)A frequency divider as claimed in claim 1, wherein a controllable switch is coupled to asaid first dataset input of the first slip-flop and tofurther comprises a third output Qa2 coupled to said controllable switch, wherein andsaid controllable switch being controlled by the clock signal driving the first flip-flop.

4. (Currently Amended)A frequency divider as claimed in claim 1, wherein the second flip-flop further comprises a third output, and wherein a controllable switch is coupled to a third output via resistive means.

REMARKS

Entry of this amendment, reconsideration and withdrawal of all grounds of objection and rejection, and allowance of the pending claims are respectfully requested in light of the above amendments and the following remarks. Claims 1-4, as amended, remain pending herein.

With regard to the drawing objections, Applicant respectfully submits that FIGs. 3 and 4 clearly show the second flip-flop has a third output Qa2. Applicant respectfully submits that the original specification, as well as U.S. Patent Application Publication 2007/0146021 A1 of this invention, discloses on page 2, paragraph [0019] a third output Qa2 shown in FIGs. 2 and 3. Accordingly, Applicant respectfully submits that no correction of the drawings is required as the claimed "third output" is clearly shown in the drawings (as well as the switch M7 and resistive means R). Reconsideration and withdrawal of this ground of objection are respectfully requested.

Applicant has amended the claims to overcome the rejections under 35 U.S.C. §112, second paragraph.

Claims 1-4 are rejected under 35 U.S.C. §102(b) over Applicant's Prior art FIGs. 1 and 2. Claims 1-2 are rejected under 35 U.S.C.§103(a) over Murray (EP 270191) in view of Edwards (U.S. 2005/0156643). Applicant respectfully traverses these grounds of rejection for the reasons indicated herein below.

With regard to the rejections under 35 U.S.C. §102(b), claim 1 has been amended to recite in part:

wherein said frequency divider does not have an additional controlled inverter for providing a time delay.

Support for the above amendment to claim 1 is clearly found in the specification at page 1, paragraph [0008] of U.S. Pat. Application Pub. 2007/0146021.

Applicant respectfully submits that FIGs. 1 and 2 of the prior art clearly show an additional controlled inverter "M5, M6" that is not present in the claimed invention.

In fact, the claimed invention is an improvement over prior art FIGs. 1 and 2 because the additional controlled inverter M5, M6 is eliminated. Applicant respectfully submits that the claimed invention is clearly not anticipated by prior art FIGs. 1 and 2, as the functions of the prior art circuits are performed with fewer elements in the claimed invention. Also, Prior Art FIGs.1 and 2 clearly do not anticipate the negative limitation recited in claim 1 about the additional controlled inverter. Nor would the combination of elements, as recited in claims 1-4, have been obvious as being within the ordinary level of skill in the art. Reconsideration and withdrawal of this ground of rejection of claims 1-4 are respectfully requested.

With regard to the rejections of claim 1 and 2 under 35 U.S.C. §103(a), Applicant respectfully submits that none of the present claims would have been obvious at the time of invention over the combination of Murray and Edwards. With regard to the combination, the recitation in claim 1 of "wherein said frequency divider does not have an additional controlled inverter for providing a time delay" is not met by the combination of references, as Murray in combination with Edwards clearly discloses that pulse train 3 is input to **delay circuit** 4 "**which delays** the pulse train applied to the clock input C of flip-flop 2 to provide a given phase relationship" (Abstract of Murray). Thus,

the combination of Murray and Edwards fails as a combination to disclose or render obvious any of the present claims.

In addition, Applicant also respectfully submits that none of the combinations of elements, as recited in any of claims 1-4 would have been obvious as being within the ordinary level of skill in the art (*KSR International v. Teleflex*, 127 S. Ct. 1727, 82 USPQ2d 1385 (2007)).

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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